Paper to discuss: *Eva-CAM: A Circuit/Architecture-Level Evaluation Tool for General Content Addressable Memories*

The general topic the paper is studying is content addressable memory (CAM), a type of memory architecture that is addressable by both the address and the contents, used to speedup searching through memory. The specific activity studied by the paper is evaluation of PPA (power, performance, and area) metrics on CAM being challenging to perform. The central research question of the paper is “For this memory architecture, evaluating different CAM design options for a given application is becoming more challenging. This paper presents Eva-CAM, a circuit/architecture-level modeling and evaluation tool for CAMs” [1].

The problem addressed by the paper is the lack of a cost and time efficient way to evaluate the PPA metrics of CAM architectures. While fabrication and HSPICE simulations are available, these methods both contain high barriers to entry for the CAM design space. Fabrication is timely, expensive, and requires access to the proper design and verification software. HSPICE simulations also require access to this software and can take days to run for accurate metrics.

The paper claims that Eva-CAM runs quickly, is accurate enough, and provides guidance as to whether a given CAM design is practical with PPA concerns for multiple nonvolatile memory (NVM) devices and design types. The supported NVM devices include resistive random access memory (RRAM), phase change memory (PCM), magnetic tunnel junction RAM (MRAM), and ferroelectric field-effect transistors (FeFET). The supported CAM designs include ternary CAM (TCAM), analog CAM (ACAM), and multi-bit CAM (MCAM).

The evidence is presented by comparing results from Eva-CAM with given input parameters with those of state-of-the-art fabricated chips and HSPICE simulations. A case study on FeFET based CAM is provided as well to show Eva-CAM’s capabilities in exploring the CAM design space.

The statistical analysis performed is a calculation of the error between Eva-CAM and the aforementioned state-of-the-art fabricated chips and HSPICE simulations.

Citation:

[1] L. Liu et al., "Eva-CAM: A Circuit/Architecture-Level Evaluation Tool for General Content Addressable Memories," 2022 Design, Automation & Test in Europe Conference & Exhibition (DATE), Antwerp, Belgium, 2022, pp. 1173-1176, doi: 10.23919/DATE54114.2022.9774572. keywords: {Semiconductor device modeling;Semiconductor device measurement;Associative memory;Nonvolatile memory;Simulation;Data models;Cams},